AmZ8136

Eight-Bit Decoder With Control Storage

DISTINCTIVE CHARACTERISTICS

- 8-bit decoder/demultiplexer with control storage
- 3-state outputs
- Common clock enable
- Common clear
- Polarity control
- Advanced Low Power Schottky Process
- 100% product assurance screening to MIL-STD-883 requirements

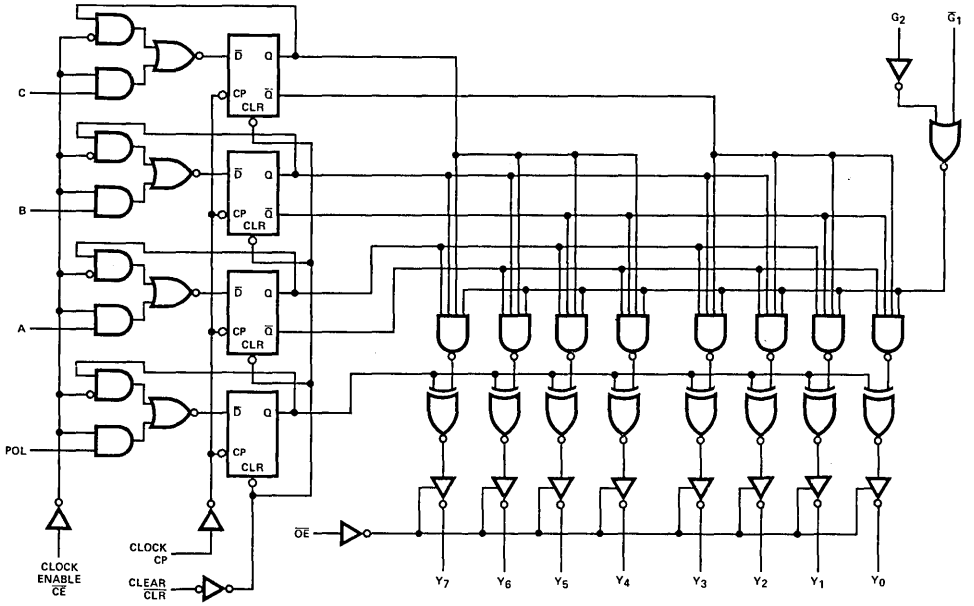
FUNCTIONAL DESCRIPTION

The AmZ8136 is an eight-bit decoder with control storage. It provides a conventional 8-bit decoder function with two enable inputs which may also be used for data input. This can be used to implement a demultiplexer function. In addition, the "exclusive-OR" gates provide polarity control of the selected output. The 3-state outputs are enabled by an active LOW input on the output enable, $\overline{OE}$.

The three control bits representing the output selection and the single bit polarity control are stored in "D" type flip-flops. These flip-flops have Clear, Clock, and Clock Enable functions provided. The $\overline{G}_1$ and G_2 inputs provide either polarity for input control or data.

LOGIC DIAGRAM

8-Bit Decoder/Demultiplexer with Control Storage



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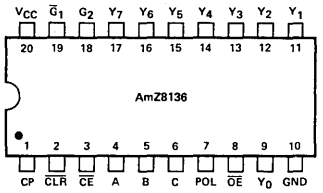
CONNECTION DIAGRAM



Note: Pin 1 is marked for orientation.

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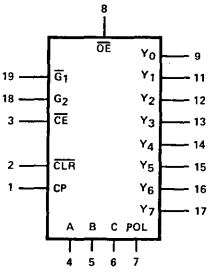
LOGIC SYMBOL



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VCC = 20
GND = 10

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75 V	MAX. = 5.25 V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50 V	MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -2.6mA$, COM'L	2.4	3.2		Volts
			$I_{OH} = -1.0mA$, MIL	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 24mA$, COM'L		0.4	0.5	Volts
			$I_{OL} = 12mA$, MIL		0.35	0.4	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$				−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$				0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$			−20	μA
			$V_O = 2.4V$			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			37	56	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test Conditions: A = B = C = $\overline{G_1}$ = G_2 = $\overline{OE}$ = $\overline{CE}$ = GND; CLK = $\overline{CLR}$ = POL = 4.5V.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	$\overline{G_1}$ to Y_0 – Y_7			17	25	ns	C_L = 45pF, R_L = 667Ω
t_{PLH}				23	34		
t_{PLH}	G_2 to Y_0 – Y_7			20	30	ns	
t_{PHL}				26	39		
t_{PLH}	CP to Y_0 – Y_7			24	36	ns	
t_{PHL}				30	45		
t_{PLH}	$\overline{CLR}$ to Y_0 – Y_7			24	36	ns	
t_{PHL}				31	46		
t_s	$\overline{CE}$ to CP		25			ns	
t_h			0				
t_s	A, B, C, POL to CP		15			ns	
t_h			0				
t_{HZ}	$\overline{OE}$ to Y_0 – Y_7			9	14	ns	C_L = 5pF, R_L = 667Ω
t_{LZ}				11	17		
t_{ZH}	$\overline{OE}$ to Y_0 – Y_7			15	22	ns	C_L = 45pF, R_L = 667Ω
t_{ZL}				16	24		
t_s	Set-up Time, Clear Recovery to CP		20			ns	
t_{pw}	Pulse Width	Clock	15			ns	
		Clear	15				

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	COM'L Max.	MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	MIL Max.	Units	Test Conditions
t_{PLH}	$\overline{G_1}$ to Y_0 – Y_7			29		31	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}				39		42		
t_{PLH}	G_2 to Y_0 – Y_7			34		37	ns	
t_{PHL}				44		48		
t_{PLH}	CP to Y_0 – Y_7			40		42	ns	
t_{PHL}				51		55		
t_{PLH}	$\overline{CLR}$ to Y_0 – Y_7			47		54	ns	
t_{PHL}				58		66		
t_s	$\overline{CE}$ to CP		27		30		ns	
t_h			0		0			
t_s	A, B, C, POL to CP		17		20		ns	
t_h			0		0			
t_{HZ}	$\overline{OE}$ to Y_0 – Y_7			17		18	ns	C_L = 5.0pF, R_L = 667Ω
t_{LZ}				27		34		
t_{ZH}	$\overline{OE}$ to Y_0 – Y_7			25		27	ns	C_L = 5.0pF, R_L = 667Ω
t_{ZL}				28		30		
t_s	Set-up Time, Clear Recovery to CP		23		25		ns	
t_{pw}	Pulse Width	Clock	17		20		ns	
		Clear	15		15			

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

FUNCTION TABLE

Mode	Inputs									Internal Registers				Three-State Outputs							
	C	B	A	POL	$\overline{CE}$	$\overline{CLR}$	G*	$\overline{OE}$	CP	Q_C	Q_B	Q_A	Q_{POL}	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
Clear	X	X	X	X	X	L	L	L	X	L	L	L	L	H	H	H	H	H	H	H	H
	X	X	X	X	X	L	H	L	X	L	L	L	L	L	H	H	H	H	H	H	H
Hold	X	X	X	X	H	H	NC	L	↑	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
Select	L	L	L	H	L	H	H	L	↑	L	L	L	H	H	L	L	L	L	L	L	L
	L	L	H	H	L	H	H	L	↑	L	L	H	H	L	H	L	L	L	L	L	L
	L	H	L	H	L	H	H	L	↑	L	H	L	H	L	L	H	L	L	L	L	L
	L	H	H	H	L	H	H	L	↑	L	H	H	H	L	L	L	H	L	L	L	L
	H	L	L	H	L	H	H	L	↑	H	L	L	H	L	L	L	L	H	L	L	L
	H	L	H	H	L	H	H	L	↑	H	L	H	H	L	L	L	L	L	H	L	L
	H	H	L	H	L	H	H	L	↑	H	H	L	H	L	L	L	L	L	L	H	L
	H	H	H	H	L	H	H	L	↑	H	H	H	H	L	L	L	L	L	L	L	H
	L	L	L	L	L	H	H	L	↑	L	L	L	L	L	H	H	H	H	H	H	H
	L	L	H	L	L	H	H	L	↑	L	L	H	L	H	L	H	H	H	H	H	H
	L	H	L	L	L	H	H	L	↑	L	H	L	L	H	H	L	H	H	H	H	H
	L	H	H	L	L	H	H	L	↑	L	H	H	L	H	H	H	L	H	H	H	H
	H	L	L	L	L	H	H	L	↑	H	L	L	L	H	H	H	H	L	H	H	H
	H	L	H	L	L	H	H	L	↑	H	L	H	L	H	H	H	H	H	L	H	H
	H	H	L	L	L	H	H	L	↑	H	H	L	L	H	H	H	H	H	H	L	H
	H	H	H	L	L	H	H	L	↑	H	H	H	L	H	H	H	H	H	H	H	L
	X	X	X	H	L	H	L	L	↑	X	X	X	H	L	L	L	L	L	L	L	L
	X	X	X	L	L	H	L	L	↑	X	X	X	L	H	H	H	H	H	H	H	H
Output Disable	X	X	X	X	X	X	X	H	X	NC	NC	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z

*

$\overline{G_1}$	G_2	G
L	L	L
L	H	H
H	L	L
H	H	L

NC = No Change X = Don't Care Z = High-Impedance ↑ = Low-to-High Transition

DEFINITION OF TERMS

$\overline{CLR}$ CLEAR – When the CLEAR input is LOW, the control register outputs (Q_A, Q_B, Q_C, Q_{POL}) are set LOW regardless of any other inputs.

CP CLOCK – Enters data into the control register on the LOW-to-HIGH transition.

$\overline{CE}$ CLOCK ENABLE – Allows data to enter the control register when $\overline{CE}$ is LOW. When $\overline{CE}$ is HIGH, the Q_i outputs do not change state, regardless of data or clock input transitions.

A,B,C Inputs to the control register which are entered on the LOW-to-HIGH clock transition if $\overline{CE}$ is LOW.

POL Input to the control register bit used for determining the polarity of the selected output.

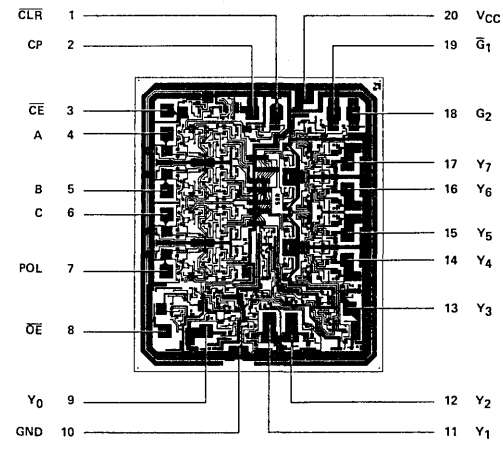
$\overline{G}_1$ Active LOW part of the expression $G = G_1G_2$ [or $G = (\overline{G}_1)G_2$] where G is either data input for the selected Y_n or is used as an input enable.

G_2 Active HIGH part of the expression $G = G_1G_2$.

Y_n The three-state outputs. When active ($\overline{OE}$ = LOW), one of eight outputs is selected by the code stored in the control register, with the polarity of all eight determined by the bit stored in the POL flip-flop of the control register. The selected output can further be controlled by G according to the expression $Y_{SELECTED} = \overline{G \oplus Q_{POL}}$.

$\overline{OE}$ OUTPUT ENABLE. When $\overline{OE}$ is HIGH the Y_n outputs are in the high impedance state; when $\overline{OE}$ is LOW the Y_n's are in their active state as determined by the other control logic. The $\overline{OE}$ input affects the Y_n output buffers only and has no effect on the control register or any other logic.

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.084" X 0.099"

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